● OVERALL BLOCK DIAGRAM

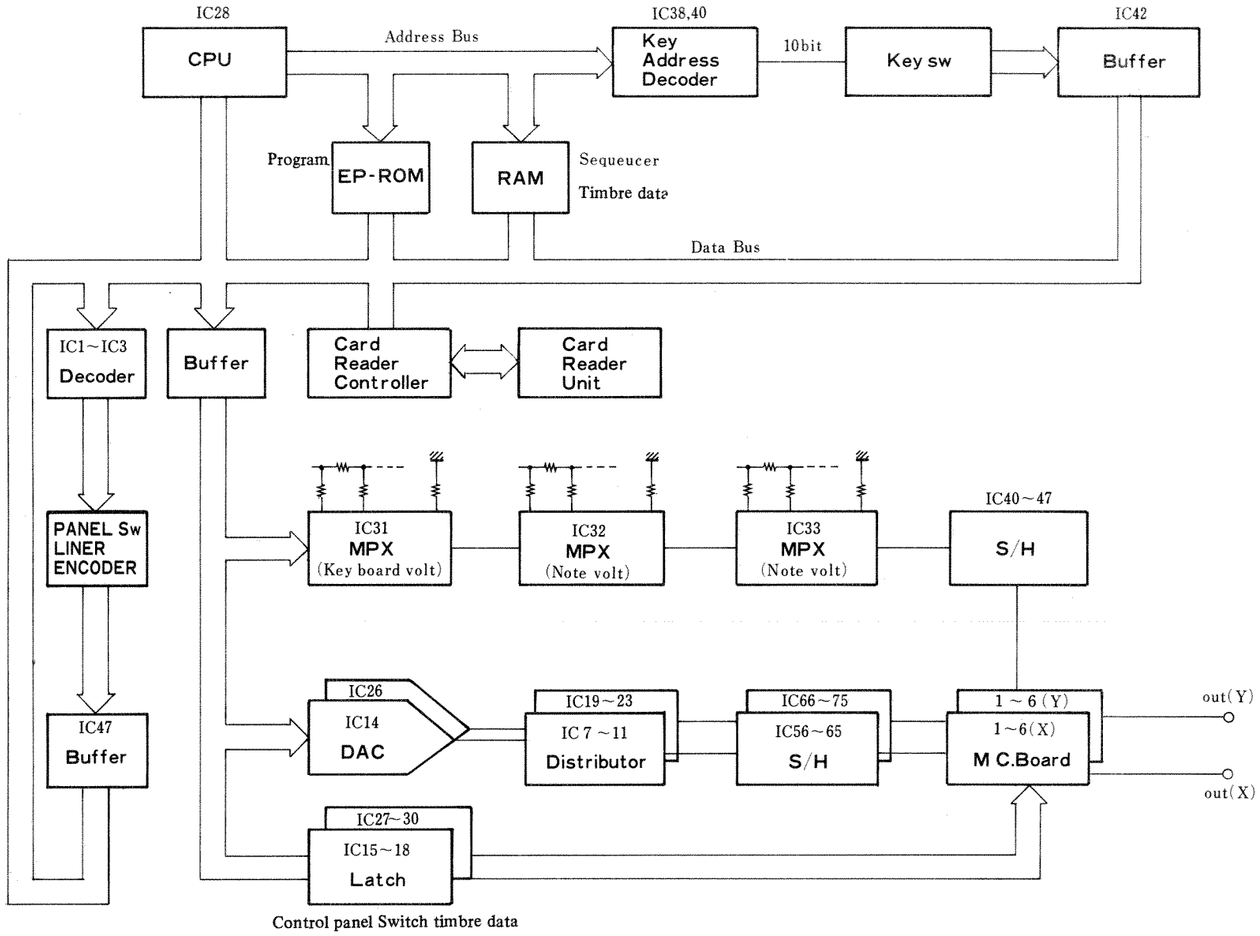


Fig. 2

● M Circuit Board Block Diagram

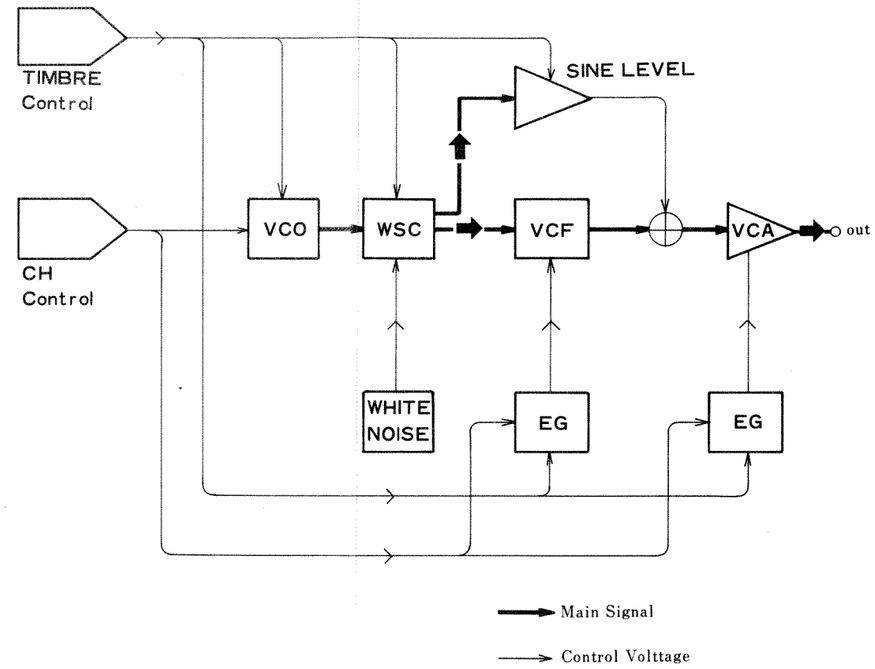


Fig. 3

2. INDIVIDUAL CIRCUIT DESCRIPTIONS

Refer to the Service Manual circuit diagrams and the overall diagram.

Keyboard Scanning Circuit (Service Manual pp. 32 ~ 34, 70, 71)

Unlike conventional synthesizers, the keyboard scanning circuit in the CS70M involves an initial passing of 3-bit address signals from the CPU to the IC38/IC40 keyboard address decoder for addressing. The decoder used here is an IC chip where low level outputs are obtained only when the enable input G1 = H and G2A = G2B (see Table 3). Furthermore, this output is switched to low voltage in succession, generating 10 scanning bits by using another IC chip.

This 10-bit output voltage is then inverted by the data bus buffer, and applied to the respective half-octave terminals of the manual keyboard. If any of the keys is then turned on under these conditions, the key switch is short circuited, and the scanning result subsequently appears at the N1 ~ N7 terminals via a diode circuit.

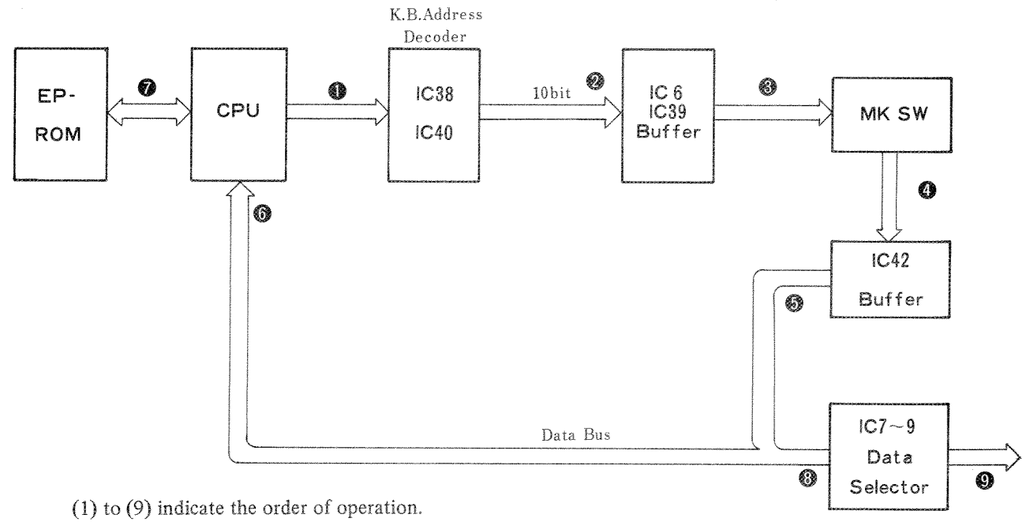
Decoder Table (for IC single-chip)

Enable		Address Input	Output							
G_1	G_{2A}	C B A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	L	L L L	L	H	H	H	H	H	H	H
H	L	L L H	H	L	H	H	H	H	H	H
H	L	L H L	H	H	L	H	H	H	H	H
H	L	L H H	H	H	H	L	H	H	H	H
H	L	H L L	H	H	H	H	L	H	H	H
H	L	H L H	H	H	H	H	H	L	H	H
H	L	H H L	H	H	H	H	H	H	L	H
H	L	H H H	H	H	H	H	H	H	H	L

Table 3

Octaves and notes are thus scanned by the KBD0 ~ KBD9 and N1 ~ N7 terminal matrix, and the results passed to the CPU via the CPU data bus. The CPU addresses key code data in the EP-ROM on the basis of the data bus results, the key code finally being passed to the data selector via the data bus. These steps are summarized in the block diagram in Fig. 4.

● Key board Scan. Block Diagram



(1) to (9) indicate the order of operation.

Fig. 4